Gliederung der Vorlesung

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Power Management – AT91

Es gibt zwei Takte auf dem Board, den System-Takt (CPU) und den Peripherie-Takt.

Grundeinstellung:

Takt für CPU	ist beim Reset **ein**geschaltet
Takt für Peripherie	ist beim Reset **aus**geschaltet

Power Management – AT91 – Memory Map

Offset	Register	Name	Access	Reset State
0x00	System Clock Enable Register	PMC_SCER	Write only	-
0x04	System Clock Disable Register	PMC_SCDR	Write only	-
0x08	System Clock Status Register	PMC_SCSR	Read only	0x1
0x0C	Reserved			
0x10	Peripheral Clock Enable Register	PMC_PCER	Write only	-
0x14	Peripheral Clock Disable Register	PMC_PCDR	Write only	-
0x18	Peripheral Clock Status Register	PMC_PCSR	Read only	0x0

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	PIOB	PIOA	-	TC5	TC4	TC3	TC2
7	6	5	4	3	2	1	0
TC1	TC0	SPI	US2	US1	US0	-	-

Layout des Peripherie Clock Registers

Power Management – AT91 – Code

Ansprechen des Peripheral Clock Enable Register mit hardcodierten Speicheradressen:

```
#define PMC_PCER        ((volatile unsigned int *) 0xFFFF4010)
int main(void) {
*PMC_PCER = 0x4200; // Peripheral Clock für PIOB einschalten
. . .
}
```

```
typedef volatile unsigned int at91_reg ;
typedef struct {
at91_reg PMC_SCER ;  // System Clock Enable  Register
at91_reg PMC_SCDR ;  // System Clock Disable Register
at91_reg PMC_SCSR ;  // System Clock Status  Register
at91_reg Reserved0 ;
at91_reg PMC_PCER ;  // Peripheral Clock Enable Reg.
at91_reg PMC_PCDR ;  // Peripheral Clock Disable Reg.
at91_reg PMC_PCSR ;  // Peripheral Clock Status Reg.
} StructPMC ;
#define PMC_BASE (( StructPMC *) 0xFFFF4000)
int main(void) {
        StructPMC* pmcbase = PMC_BASE; // Basisadresse PMC
        pmcbase->PMC_PCER= 0x4200;     // Peripheral Clocks einschalten
                                       // für PIOB Komponenten _____,
```

Power Management – SAM3X PMC Memory Map

Offset	Register	Name	Access	Reset
0x00	System Clock Enable Register	PMC_SCER	write only	-
0x04	System Clock Disable Register	PMC_SCDR	write only	-
0x08	System Clock Status Register	PMC_SCSR	read only	1
	....			
0x10	Peripheral Clock Enable Register 0	PMC_PCER0	write only	-
0x14	Peripheral Clock Disable Register 0	PMC_PCDR0	write only	-
0x18	Peripheral Clock Status Register 0	PMC_PCSR0	read only	0
	....			
	....			
0x100	Peripheral Clock Enable Register 1	PMC_PCER1	write only	-
0x104	Peripheral Clock Disable Register 1	PMC_PCDR1	write only	-
0x108	Peripheral Clock Status Register 1	PMC_PCSR1	read only	0
	....			

vergleiche Tabelle 28-3

Power Management – SAM3X – Register Layout

31	30	29	28	27	26	25	24
TC4	TC3	TC2	TC1	TC0			
23	22	21	20	19	18	17	16
					USART0		
15	14	13	12	11	10	9	8
	PIOD	PIOC	PIOB	PIOA			
7	6	5	4	3	2	1	0
							....

PMC 0

PMC->PMC_PCER0 = 0x1 << 27; PMC->PMC_PCER0 = PMC_PCER0_PID27;

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
			....	TC8 (35)	TC7 (34)	TC6 (33)	TC5 (32)

PMC 1

Peripheral Identifiers

PMC->PMC_PCER1 = 0x1 << 3; PMC->PMC_PCER1 = PMC_PCER1_PID35;

Power Management – SAM3X – Peripheral Clock

28.15.4 PMC Peripheral Clock Enable Register 0

Name: PMC_PCER0

Address: 0x400E0610

Access: Write-only

31	30	29	28	27	26	25	24
PID31	PID30	PID29	PID28	PID27	PID26	PID25	PID24
23	22	21	20	19	18	17	16
PID23	PID22	PID21	PID20	PID19	PID18	PID17	PID16
15	14	13	12	11	10	9	8
PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
7	6	5	4	3	2	1	0
PID7	PID6	PID5	PID4	PID3	PID2	–	–

This register can only be written if the WPEN bit is cleared in "PMC Write Protect Mode Register" .

- **PIDx: Peripheral Clock x Enable**

0 = No effect.

1 = Enables the corresponding peripheral clock.

Note: To get PIDx, refer to identifiers as defined in the section "Peripheral Identifiers" in the product datasheet. Other peripherals can be enabled in PMC_PCER1 (Section 28.15.23 "PMC Peripheral Clock Enable Register 1").

Note: Programming the control bits of the Peripheral ID that are not implemented has no effect on the behavior of the PMC.

28.15.23 PMC Peripheral Clock Enable Register 1

Name: PMC_PCER1

Address: 0x400E0700

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	PID44	PID43	PID42	PID41	PID40
7	6	5	4	3	2	1	0
PID39	PID38	PID37	PID36	PID35	PID34	PID33	PID32

This register can only be written if the WPEN bit is cleared in "PMC Write Protect Mode Register" .

- **PIDx: Peripheral Clock x Enable**

0 = No effect.

1 = Enables the corresponding peripheral clock.

Notes: 1. To get PIDx, refer to identifiers as defined in the section "Peripheral Identifiers" in the product datasheet.
2. Programming the control bits of the Peripheral ID that are not implemented has no effect on the behavior of the PMC.

Peripheral IDs (PID) sind eindeutige Nummern, die jeweils einer Peripheriekomponente zugeordnet ist. Der SAM3X erlaubt es bei der weiteren Konfiguration, zwischen PIDs zu wählen, die einem Ein-/Ausgangspin zugeordnet werden sollen.

Power Management – PIDs

Table 9-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	X		Supply Controller
1	RSTC	X		Reset Controller
2	RTC	X		Real-time Clock
3	RTT	X		Real-time Timer
4	WDG	X		Watchdog Timer
5	PMC	X		Power Management Controller
6	EEFC0	X		Enhanced Embedded Flash Controller 0
7	EEFC1	X		Enhanced Embedded Flash Controller 1
8	UART	X		Universal Asynchronous Receiver Transceiver
9	SMC_SDRAMC	X	X	Static Memory Controller / Synchronous Dynamic RAM Controller
10	SDRAMC	X		Synchronous Dynamic RAM Controller
11	PIOA	X	X	Parallel I/O Controller A
12	PIOB	X	X	Parallel I/O Controller B
13	PIOC	X	X	Parallel I/O Controller C
14	PIOD	X	X	Parallel I/O Controller D
15	PIOE	X	X	Parallel I/O Controller E
16	PIOF	X	X	Parallel I/O Controller F
17	USART0	X	X	Universal Synchronous Asynchronous Receiver Transmitter 0
18	USART1	X	X	Universal Synchronous Asynchronous Receiver Transmitter 1
19	USART2	X	X	Universal Synchronous Asynchronous Receiver Transmitter 2
20	USART3	X	X	Universal Synchronous Asynchronous Receiver Transmitter 3
21	HSMCI	X	X	High Speed Multimedia Card Interface
22	TWI0	X	X	Two-Wire Interface 0
23	TWI1	X	X	Two-Wire Interface 1
24	SPI0	X	X	Serial Peripheral Interface 0
25	SPI1	X	X	Serial Peripheral Interface 1
26	SSC	X	X	Synchronous Serial Controller
27	TC0	X	X	Timer Counter Channel 0
28	TC1	X	X	Timer Counter Channel 1
29	TC2	X	X	Timer Counter Channel 2

Table 9-1. Peripheral Identifiers (Continued)

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
30	TC3	X	X	Timer Counter Channel 3
31	TC4	X	X	Timer Counter Channel 4
32	TC5	X	X	Timer Counter Channel 5
33	TC6	X	X	Timer Counter Channel 6
34	TC7	X	X	Timer Counter Channel 7
35	TC8	X	X	Timer Counter Channel 8
36	PWM	X	X	Pulse Width Modulation Controller
37	ADC	X	X	ADC Controller
38	DACC	X	X	DAC Controller
39	DMAC	X	X	DMA Controller
40	UOTGHS	X	X	USB OTG High Speed
41	TRNG	X	X	True Random Number Generator
42	EMAC	X	X	Ethernet MAC
43	CAN0	X	X	CAN Controller 0
44	CAN1	X	X	CAN Controller 1

Siehe serial.c

```
// Power Management - turn on clock for USART1 (PID 18)
PMC->PMC_PCER0 = 1 << 18;
```